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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,317	11/20/2001	Xavier Mariaud	00RO27054366	9505

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,317	MARIAUD ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of the After Final Amendment filed on 21st of March 2005. Claims 5, 11, 17, 20 and 22 have been amended; no claim has been canceled; and no claim has been newly added since the Final Office Action was mailed on 21st of December 2004.

2. Receipt is acknowledged of the request filed on 19th of April 2005 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/989,317, which the request is acceptable and an RCE has been established. Currently, claims 5-22 are pending in this application.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 5-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Saito et al. [US 5,019,966; hereinafter Saito].

Referring to claim 5, AAPA discloses a computer system (See Fig. 1) comprising:

- a master apparatus (i.e., Master Apparatus A in Fig. 1); and
- a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with said master apparatus (See page 1, lines 10-22) and communicating via a universal serial bus (USB) protocol (See page 1, lines 22-25), said slave apparatus comprising
    - a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3*),

* See the specification pages 2-3, Background of the Invention.

- a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7[†]),
- a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit), and
- an interruption state latch (i.e., a flag CTR in Fig. 3(d)) and a control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) cooperating therewith for supplying an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) to said microprocessor (See page 3, lines 14-20; i.e., wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)).

[†] See the specification page 6, line 33 through page 8, line 7, the Applicants admit the portion as a prior art, i.e., about the existing system.

AAPA does not teach that said interruption signal has been recorded by said sending/receiving circuit when said microprocessor is unavailable.

Saito discloses a data transmission/reception apparatus (See Abstract and Fig. 8), wherein a slave apparatus (i.e., second serial data processor 410 of Fig. 8; See col. 11, lines 56-59) comprising

- an interruption state latch (i.e., means for issuing Shift Clock 363 of Serial Clock Controller 312 in Fig. 8) and a control circuit cooperating therewith (i.e., Serial Clock Controller 312 of Fig. 8) for supplying an interruption signal (i.e., Serial Interrupt Signal 361 of Fig. 8) to a microprocessor (i.e., Data Processing Unit 316 of Fig. 8) once the start of a new message has been acknowledged and recorded by a sending/receiving circuit (i.e., after having received 8-bit serial data into Shift Register 311 of Fig. 8, said Serial Interrupt Signal is issued at t_{21} to said Data Processing Unit in Fig. 9; See col. 13, lines 2-4) when[‡] said microprocessor is unavailable (i.e., during said Data Processing Unit is busy for processing Main Program till t_{21} of the Serial Clock 352 in Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined said interruption state latch and a control circuit, as disclosed by Saito, with said interruption state latch (i.e., a flag CTR) and a control circuit (i.e., means for controlling said flag CTR), as disclosed by AAPA, for the advantage of providing said microprocessor of slave apparatus (i.e., data processor) which can be used as a receiver and which can generate said microprocessor unavailable signal (i.e., busy signal) without requiring a special program, so that said microprocessor (i.e., data processor) can process said interrupt signal (i.e., interrupt) generated in said microprocessor unavailable condition (i.e., busy condition; See Saito, col. 2, lines 29-33).

Referring to claim 6, AAPA teaches said control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) for controlling said interruption state latch (See page 3, lines 14-26) comprises

[‡] cf. Merriam-Webster's Collegiate® Dictionary (10th ed.) - '*when*' is defined as 'at or during the time that : WHILE'.

- at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

Referring to claim 7, AAPA teaches

- said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) prevents said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal).

Referring to claim 8, AAPA teaches

- said master apparatus (i.e., Master Apparatus A in Fig. 1) comprises a central processing unit (i.e., Microcontroller 26 of Fig. 1).

Referring to claim 9, AAPA teaches

- said slave apparatus (i.e., Slave Apparatus B in Fig. 1) comprises computer peripheral device (See page 1, line 3-5).

Referring to claim 10, AAPA teaches

- a cable (i.e., cable 20 of Fig. 1) connecting said master apparatus and said slave apparatus (See page 1, lines 10-19).

Referring to claim 11, AAPA discloses a computer system (See Fig. 1) comprising:

- a master apparatus (i.e., Master Apparatus A in Fig. 1); and
- a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with said master apparatus (See page 1, lines 10-22) and comprising
    - a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3),
    - a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7),
    - a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of

the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit), and

- an interruption state latch (i.e., a flag CTR in Fig. 3(d)) for supplying an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) to said microprocessor (See page 3, lines 14-20; i.e., wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)),
- said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) preventing said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information from

being written into said plurality of state latches during receipt of said start of said new message and during the presence of said interruption signal).

AAPA does not teach that said interruption signal has been recorded by said sending/receiving circuit when said microprocessor is unavailable.

Saito discloses a data transmission/reception apparatus (See Abstract and Fig. 8), wherein a slave apparatus (i.e., second serial data processor 410 of Fig. 8; See col. 11, lines 56-59) comprising

- an interruption state latch (i.e., Serial Clock Controller 312 of Fig. 8) for supplying an interruption signal (i.e., Serial Interrupt Signal 361 of Fig. 8) to a microprocessor (i.e., Data Processing Unit 316 of Fig. 8) once the start of a new message has been acknowledged and recorded by a sending/receiving circuit (i.e., after having received 8-bit serial data into Shift Register 311 of Fig. 8, said Serial Interrupt Signal is issued at t_{21} to said Data Processing Unit in Fig. 9; See col. 13, lines 2-4) when[§] said microprocessor is unavailable (i.e., during said Data Processing Unit is busy for processing Main Program till t_{21} of the Serial Clock 352 in Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined said interruption state latch, as disclosed by Saito, with said interruption state latch (i.e., a flag CTR), as disclosed by AAPA, for the advantage of providing said microprocessor of slave apparatus (i.e., data processor) which can be used as a receiver and which can generate said microprocessor unavailable signal (i.e., busy signal) without requiring a special program, so that said microprocessor (i.e., data processor) can process said interrupt signal (i.e., interrupt) generated in said microprocessor unavailable condition (i.e., busy condition; See Saito, col. 2, lines 29-33).

Referring to claim 12, AAPA teaches

[§] cf. Merriam-Webster's Collegiate® Dictionary (10th ed.) - '*when*' is defined as 'at or during the time that : WHILE'.

- said master apparatus and said slave apparatus communicate via a universal serial bus (USB) protocol (See page 1, lines 22-25).

Referring to claim 13, AAPA teaches

- at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

Referring to claim 14, AAPA teaches

- said master apparatus (i.e., Master Apparatus A in Fig. 1) comprises a central processing unit (i.e., Microcontroller 26 of Fig. 1).

Referring to claim 15, AAPA teaches

- said slave apparatus (i.e., Slave Apparatus B in Fig. 1) comprises computer peripheral device (See page 1, line 3-5).

Referring to claim 16, AAPA teaches

- a cable (i.e., cable 20 of Fig. 1) connecting said master apparatus and said slave apparatus (See page 1, lines 10-19).

Referring to claim 17, AAPA discloses a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1; See page 1, lines 10-22) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said slave apparatus comprising:

- a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3);
- a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7);
- a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing.said binary information received by said sending/receiving circuit); and
- an interruption state latch (i.e., a flag CTR in Fig. 3(d)) and a control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) cooperating therewith for supplying an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) to said microprocessor (See page 3, lines

14-20; i.e., wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)).

AAPA does not teach that said interruption signal has been recorded by said sending/receiving circuit when said microprocessor is unavailable.

Saito discloses a data transmission/reception apparatus (See Abstract and Fig. 8), wherein a slave apparatus (i.e., second serial data processor 410 of Fig. 8; See col. 11, lines 56-59) comprising

- an interruption state latch (i.e., Serial Clock Controller 312 of Fig. 8) for supplying an interruption signal (i.e., Serial Interrupt Signal 361 of Fig. 8) to a microprocessor (i.e., Data Processing Unit 316 of Fig. 8) once the start of a new message has been acknowledged and recorded by a sending/receiving circuit (i.e., after having received 8-bit serial data into Shift Register 311 of Fig. 8, said Serial Interrupt Signal is issued at t_{21} to said Data Processing Unit in Fig. 9; See col. 13, lines 2-4) when** said microprocessor is unavailable (i.e., during said Data Processing Unit is busy for processing Main Program till t_{21} of the Serial Clock 352 in Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined said interruption state latch, as disclosed by Saito, with said interruption state latch (i.e., a flag CTR), as disclosed by AAPA, for the advantage of providing said microprocessor of slave apparatus (i.e., data processor) which can be used as a receiver and which can generate said microprocessor unavailable signal (i.e., busy signal) without requiring a special program, so that said microprocessor (i.e., data processor) can process said interrupt signal (i.e., interrupt) generated in said microprocessor unavailable condition (i.e., busy condition; See Saito, col. 2, lines 29-33).

** cf. Merriam-Webster's Collegiate® Dictionary (10th ed.) - '*when*' is defined as 'at or during the time that : WHILE'.

Referring to claim 18, AAPA teaches said control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) for controlling said interruption state latch (See page 3, lines 14-26) comprises

- at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

Referring to claim 19, AAPA teaches

- said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) prevents said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal).

Referring to claim 20, AAPA discloses a method of processing interruptions (See page 3, lines 14-26) in a slave apparatus (i.e., Slave Apparatus B in Fig. 1) communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said method comprising:

- sending and receiving binary information to and from said master apparatus via a sending/receiving circuit (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3);
- generating state signals of said sending/receiving circuit based upon said status signals (See page 7, line 18 through page 8, line 7);
- processing applications of said slave apparatus (i.e., SW Process 'main routine' in Fig. 3(e)) and also processing said binary information received by said sending/receiving circuit (See page 3, lines 24-26); and
- supplying an interruption signal (i.e., CTR being set to '1' in Fig. 3(d)) to a microprocessor of said slave apparatus (i.e., Microcontroller 28 of said Slave Apparatus B in Fig. 1; See page 3, lines 14-20, wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)).

AAPA does not teach that said interruption signal has been recorded by said sending/receiving circuit when said microprocessor is unavailable.

Saito discloses a data transmission/reception apparatus (See Abstract and Fig. 8), wherein a data transferring method (See col. 1, lines 10-13) comprising

- supplying an interruption signal (i.e., Serial Interrupt Signal 361 of Fig. 8) to a microprocessor of a slave apparatus (i.e., Data Processing Unit 316 of second serial data processor 410 in Fig. 8; See col. 11, lines 56-59) once the start of a new message has been acknowledged and recorded by a sending/receiving circuit (i.e., after having received 8-bit serial data into Shift Register 311 of Fig. 8, said Serial Interrupt Signal is issued at t_{21} to said Data Processing Unit in Fig. 9; See col. 13, lines 2-4) when[††] said microprocessor is unavailable (i.e., during said Data Processing Unit is busy for processing Main Program till t_{21} of the Serial Clock 352 in Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined said data transferring method, as disclosed by Saito, with said method step of supplying said interruption signal, as disclosed by AAPA, for the advantage of providing said microprocessor of slave apparatus (i.e., data processor) which can be used as a receiver and which can generate said microprocessor unavailable signal (i.e., busy signal) without requiring a special program, so that said microprocessor (i.e., data processor) can process said interrupt signal (i.e., interrupt) generated in said microprocessor unavailable condition (i.e., busy condition; See Saito, col. 2, lines 29-33).

Referring to claim 21, AAPA teaches

- supplying said interruption signal comprises setting an interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) based upon said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) to indicate a microprocessor interruption request (See page 3, lines 14-18).

[††] cf. Merriam-Webster's Collegiate® Dictionary (10th ed.) - '*when*' is defined as 'at or during the time that : WHILE'.

Referring to claim 22, AAPA discloses a method of processing interruptions (See page 3, lines 14-26) in a slave apparatus (i.e., Slave Apparatus B in Fig. 1) communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said method comprising:

- generating a state signal indicating the end of a message (See page 1, line 26 through page 2, line 6);
- detecting a start of a new message (i.e., message 'IN' signal in Fig. 3(a)) from said master apparatus (See page 2, lines 7-10) and producing a start of message state signal (i.e., 'ready' state signal);
- recording data from the start of said new message (See page 2, lines 13-17);
- acknowledging receipt of the start of said new message (i.e., ACK signal in Fig. 3(a));
- generating a signal (i.e., flag CTR in Fig. 3(d)) indicating completion (i.e., CTR being set to '0' in Fig. 3(d)) of recordation of said data from the start of said new message (See page 3, lines 14-26); and
- generating an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) for a microprocessor of said slave apparatus (i.e., Microcontroller 28 of said Slave Apparatus B in Fig. 1; See page 3, lines 14-20, wherein in fact that an interruption of said Microcontroller being requested by USB bus clearly anticipates said interruption signal, viz., interruption request when CTR is set to '1' in Fig. 3(d), being supplied to said microprocessor) in the presence of said state signal indicating the end of said message, the start of message state signal, and said signal indicating completion of recordation of said data from the start of said new message (See page 3, lines 14-16; i.e., wherein in fact that at the end of transfer phase, an interruption of the microcontroller to process the part of the transmitted message may be requested inherently

anticipates generating an interruption signal in the presence of said state signal indicating the end of said message (i.e., CTR being set to '1'), the start of message state signal (i.e., 'ready' state signal), and said signal indicating completion of recordation of said data from the start of said new message).

AAPA does not teach that generating said interruption signal in the presence of said signal indicating completion of recordation of said data from the start of said new message when said microprocessor is unavailable.

Saito discloses a data transmission/reception apparatus (See Abstract and Fig. 8), wherein a data transferring method (See col. 1, lines 10-13) comprising

- generating an interruption signal (i.e., Serial Interrupt Signal 361 of Fig. 8) for a microprocessor of a slave apparatus (i.e., Data Processing Unit 316 of second serial data processor 410 in Fig. 8; See col. 11, lines 56-59) in the presence of a signal indicating completion of recordation of said data from the start of said new message when said microprocessor is unavailable (i.e., after having received 8-bit serial data into Shift Register 311 of Fig. 8, said Serial Interrupt Signal is issued at t_{21} to said Data Processing Unit in Fig. 9; See col. 13, lines 2-4) when[‡‡] said microprocessor is unavailable (i.e., during said Data Processing Unit is busy for processing Main Program till t_{21} of the Serial Clock 352 in Fig. 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined said data transferring method, as disclosed by Saito, with said method step of generating said interruption signal, as disclosed by AAPA, for the advantage of providing said microprocessor of slave apparatus (i.e., data processor) which can be used as a receiver and which can generate said microprocessor unavailable signal (i.e., busy signal) without requiring a special program, so

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[‡‡] cf. Merriam-Webster's Collegiate® Dictionary (10th ed.) - '*when*' is defined as 'at or during the time that : WHILE'.

that said microprocessor (i.e., data processor) can process said interrupt signal (i.e., interrupt) generated in said microprocessor unavailable condition (i.e., busy condition; See Saito, col. 2, lines 29-33).

Response to Arguments

5. Applicants' arguments with respect to claims 5, 11, 17, 10 and 22 have been considered but are moot in view of the new ground(s) of rejection.

The Examiner brought Saito et al. [US 5,019,966] reference in the rejection for the limitations which are not provided by AAPA and all of the other art cited (See *Claim Rejections - 35 USC § 103*). Furthermore, all of the other Applicants' arguments had been properly discussed in the Advisory Office Action mailed on 15th of March 2005 (paper no. 20050311).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure.

Roy et al. [US 6,134,653 A] disclose RISC processor architecture with high performance context switching in which one context can be loaded by a co-processor while another context is being accessed by an arithmetic logic unit.

Nomura et al. [US 6,606,320 B1] disclose data communication system and method, data transmission device and method.

MacDonald et al. [US 5,765,003 A] disclose interrupt controller optimized for power management in a computer system or subsystem.

Suzuki [US 5,581,770 A] discloses floating interruption handling system and method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

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